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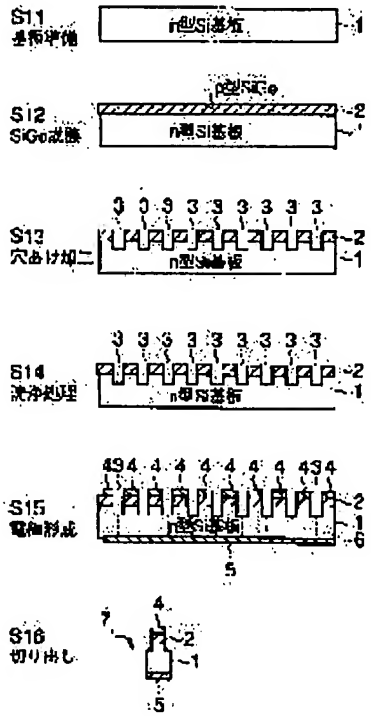
(54) METHOD FOR FABRICATING SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method for fabricating a semiconductor device in which a leakage current is not generated on the heterojunction interface of SiGe/Si.

SOLUTION: In the method for fabricating a semiconductor device having a junction interface where first conductivity type SiGe and second conductivity type Si or SiGe touch each other, the junction interface is cleaned, at the part thereof exposed to the surface, with a solution containing hydrofluoric acid and then cleaned with a solution containing sulfuric acid.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The production approach of the semiconductor device characterized by for said junction interface washing the part exposed to a front face with the solution containing hydrofluoric acid, and washing with the solution containing a sulfuric acid after that in the production approach of a semiconductor device of having the junction interface in which SiGe of the 1st conductivity type, Si of the 2nd conductivity type, or SiGe carries out mutual contact.
[Claim 2] The production approach of the semiconductor device characterized by to cover an insulating material into the part which said junction interface etched the part exposed to a front face, and washed with the solution containing hydrofluoric acid, and subsequently washed with the solution containing a sulfuric acid after that in the production approach of a semiconductor device of having the junction interface in which SiGe of the 1st conductivity type, Si of the 2nd conductivity type, or SiGe carries out mutual contact, and said junction interface has exposed subsequently to a front face.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a semiconductor device of manufacturing the diode which used SiGe, and a semiconductor device like a transistor.
[0002]
[Description of the Prior Art] Since the SiGe mixed-crystal film can realize the transistor which was excellent in the high frequency property carrying out to the electron device joined to Si, for example, the structure which carried out sequential junction of the n mold Si-p mold SiGe-n mold Si, i.e., a heterojunction mold bipolar transistor, compared with the structure of only Si, it has spread through the integrated circuit of a high frequency application widely by the end of today. Moreover, this invention person showed clearly that the recovery time amount when carrying out bias conversion from the forward direction to hard flow compared with the conventional Si diode is short, and high-speed operation is possible in the previous application specification of an application for patent No. 044306 [2000 to] and a previous drawing for the diode which joined Si of the p mold SiGe, n mold, or n-mold.
[0003] In the heterojunction mold transistor and diode using the SiGe mixed-crystal film of such a property, it is strongly requested among manufacturers from the viewpoint of the improvement in the yield, and a viewpoint of application expansion that a withstand voltage property is raised. For this reason, although the diode structure of the near part which pressure-proofing requires, i.e., the structure which joined the p mold SiGe and the n mold Si, the structure which joined the n mold SiGe and the p mold Si, and these are generically called SiGe/Si diode below, for this SiGe/Si diode, the leakage current at the time of the reverse bias in a pn junction interface poses a problem.
[0004]
[Problem(s) to be Solved by the Invention] The leakage current produced to the conventional SiGe/Si diode is explained with reference to drawing 3 . Drawing 3 is drawing having shown typically the leakage current produced when a reverse bias is applied to the SiGe/Si diode 10. If a reverse bias is applied to diode 10, a depletion layer 13 will be made like illustration in the place of a pn junction interface, and electric field will concentrate on this depletion layer 13. The part 16 exposed to the exterior of diode exists in a pn junction interface, and the depletion layer in this exposed part 16 is in the inclination for width of face to become narrow compared with the depletion layer of the other place. Therefore, the degree of electric-field concentration becomes high and the leakage current in this exposed part 16 produced to diode will be strongly governed in the matter condition of the exposed part 16.
[0005] Here, the matter conditions of the exposed part 16 which governs the leakage current are specifically the crystal defect in the exposed part 16, air discharge, and three of impurities. Among these, it depends for the crystal defect on the production process of each semi-conductor layer, and since sufficient attention is paid so that a crystal defect may not start quality control of a semi-conductor production process as much as possible, by the time it grows up to be an injurious defect if independent, to the extent that it cannot ignore, in the usual case, it will not result. Moreover, in the advanced

technology given in the application specification of an application for patent No. 025428 [2000 to], and a drawing, management of covering a surface with insulating materials, such as silicone gel, is made so that it may not happen about air discharge.

[0006] However, about an impurity, the effective solution is not former yet clarified like front 2 persons. There is an impurity which adheres at the time of atmospheric air, such as metals, such as Na, K, Fe, and Au, and a hydrocarbon, or rinsing in the impurity element which can cause the leakage current. Moreover, if the exposed part 16 oxidizes and germanium oxide is generated by the front face, this oxide will also cause the leakage current. Therefore, in order to suppress the leakage current low, in the exposed part 16, the processing which lessens enough the harmful impurity which suppressed the crystal defect, and suppressed air discharge upwards, and carries out induction of the leakage current further is required.

[0007] By the way, in the conventional diode which consists of Si altogether, it is common to carry out thermal oxidation processing of the exposed part of pn junction. If this is the approach of oxidizing the front face of diode under hot oxygen 900 degrees C or more or the ambient atmosphere of a steam and this thermal oxidation processing is performed, Si of an exposed part will oxidize, it will insulation-ize, and, thereby, the leakage current will decrease. Although such an oxidizing [thermally] method is powerless to a metal impurity, with the device of Si system, it is effective and is used frequently until now.

[0008] However, if the conventional oxidizing [thermally] method is applied to SiGe/Si diode as it is, the segregation of germanium will happen to the part of the interface of the oxidizing zone and SiGe which are made on the surface of SiGe, and this will cause the leakage current. For this reason, in order to apply the oxidizing [thermally] method to SiGe, the oxidation conditions from which germanium does not start a segregation need to be retrieval inquired careful, but a report is not yet seen until it continues up to now, but that effective policy is left behind while it has been unsolved.

[0009] In addition, although the trouble of the above-mentioned conventional technique is related with the heterojunction interface of SiGe/Si diode, the same problem is produced also for SiGe/SiGe diode.

[0010] It is made in order that this invention may solve the above-mentioned technical problem, and it aims at a SiGe/Si heterojunction interface or a SiGe/SiGe heterojunction interface, and providing especially the exposure with the production approach of the semiconductor device which does not produce the leakage current.

[0011]

[Means for Solving the Problem] It is characterized by for said junction interface washing the part exposed to a front face with the solution containing hydrofluoric acid, and washing the production approach of the semiconductor device concerning this invention with the solution containing a sulfuric acid after that in the production approach of a semiconductor device of having the junction interface in which SiGe of the 1st conductivity type, Si of the 2nd conductivity type, or SiGe carries out mutual contact.

[0012] Moreover, the production approach of the semiconductor device concerning this invention In the production approach of a semiconductor device of having the junction interface in which SiGe of the 1st conductivity type, Si of the 2nd conductivity type, or SiGe carries out mutual contact, said junction interface etches the part exposed to a front face. Subsequently The solution containing hydrofluoric acid washes, the solution containing a sulfuric acid washes after that, and it is characterized by covering an insulating material into the part which said junction interface has exposed subsequently to a front face.

[0013] If the surface exposure part of the junction interface of SiGe/Si diode is left in atmospheric air, it will oxidize automatically. At this time, mixing of adsorption of the impurities out of atmospheric air (hydrocarbon etc.), the metal (Na, K) ion brought about when an operator contacts empty-handed etc., the oxide (GeO2) of germanium made by oxidizing further, etc. are assumed as an impurity. These impurities cause the leakage current and reduce the proof-pressure property of a semiconductor device.

[0014] In this invention, SiGe/Si diode is dipped in the solution which contains hydrofluoric acid first for removing the oxide made into this exposed part. By changing the time amount which dips even the thickness of about several micrometers in a hydrofluoric acid solution as an oxidizing zone, it can

remove easily. Hydrogen termination of the junction interface is carried out by this washing processing on the front face of an exposed part. However, a hydrocarbon metallurgy group impurity is not removed at this process.

[0015] Subsequently, if SiGe/Si diode is dipped in a sulfuric-acid content water solution, a metal impurity and a hydrocarbon will melt and appear in a solution, and will be removed from a surface. In this case, although a surface oxidizes by the thickness of 1nm (10A) extent, the oxide (GeO2) of germanium is not made only from SiO2 being made in this case. Although surface germanium atom oxidizes under the effect of a sulfuric acid, since germanium oxide melts into the solution of a sulfuric acid, it does not remain in a surface as GeO2. Impurities, such as a metal, a hydrocarbon, and germanium oxide, are pressed down low, and also the condition of the surface made here can do Si oxide thinly at a surface, and has the work to which this is inactive so much from the external world to an impurity, and suppresses subsequent impurity adsorption.

[0016] Although hydrofluoric acid processing and vitriolization are performed one by one in this invention, when either is missing, the effectiveness of this invention is not discovered. While the removal of GeO2 in the natural oxidation film becomes inadequate when hydrofluoric acid processing is missing, and the surface natural oxidation film is thick, the metal impurity in the natural oxidation film is unremovable. On the other hand, when vitriolization is missing, the metal impurity and hydrocarbon which it cannot finish taking by hydrofluoric acid processing will remain. Moreover, when these hydrofluoric acid processing and vitriolization are made reverse, in order that a front face may finish with hydrogen termination, the effectiveness that a front face suppresses subsequent impurity adsorption compared with this invention finished with an oxide film becomes weak.

[0017] In SiGe/Si diode, the causes of the leakage current at the time of a reverse bias are one crystal defect in the surface exposure part of a junction interface, 2 air discharge, and three impurities, as mentioned above.

[0018] Although the 1st invention is the approach of removing a surface impurity effectively, it is adding one crystal defect and the process which removes 2 air discharge to this like the 2nd invention, and serves as diode with still less leakage current.

[0019] Specifically, it removes by etching a surface with alkali system water solutions, such as chemical etching, for example, KOH etc., the mixed water solution of fluoric acid and a nitric acid, etc. for removal of the crystal defect of a semi-conductor surface part. Thereby, the crystal defect by the surface damage by processing of a scratch blemish, the plasma, etc. can be removed. After that, in order to remove an impurity, in the hydrofluoric acid solution and sulfuric-acid solution which were shown by 1st invention, sequential immersion is carried out and it washes. Then, contact to air is prevented by covering a front face with an insulating material. By combining these three policies, SiGe/Si diode with little performance degradation by the leakage current can be obtained.

[0020] Although the above-mentioned policy explains the example of SiGe/Si diode, the same effectiveness can be acquired also for SiGe/SiGe diode.

[0021]

[Embodiment of the Invention] Hereafter, various desirable examples of this invention are explained with reference to an attached drawing.

[0022] (Example 1) The p-SiGe/n-Si junction diode was produced as a semiconductor device of an example 1. The production approach is explained with reference to drawing 1 . The Si substrate 1 of n mold of 15ohms of membrane resistance cm was prepared (process S11). Laminating formation of the SiGe film 2 of p mold was carried out on this n mold Si substrate 1 at 0.4 micrometers in thickness (process S12). A chemical-vapor-deposition method like CVD was used for membrane formation of this p mold SiGe film 2. Concentration of p mold dopant in the SiGe film 2 was made into 1017cm - three sets. Moreover, germanium concentration in the SiGe film 2 was made into pentatomic %.

[0023] subsequently, parts other than the part which it leaves as diode -- laws, such as dry etching or wet etching, -- by removing using a method, punching processing of a predetermined pattern was performed on the SiGe film 2, and many substrate exposures 3 were formed (process S13). These substrate outcrops 3 set width of face to 1mm, and set 30 micrometers and mutual pitch spacing to 1.5-5mm for

the depth.
[0024] Then, after immersing the SiGe/Si layered product into the hydrofluoric acid solution and performing 1st washing processing, it rinsed and dried, the SiGe/Si layered product was immersed into the sulfuric-acid solution, and 2nd washing processing was performed (process S14). The hydrofluoric acid solution used for the 1st washing processing dilutes the hydrofluoric acid of 48 mass % concentration to 1/50 with water. The sulfuric-acid solution used for the 2nd washing processing prepares a sulfuric-acid 96 mass % water solution and a hydrogen-peroxide-solution 48 mass % solution at a rate of 1:2.
[0025] Then, laminating formation of the metal electrodes 4 and 5 was carried out with the vacuum deposition method on the top face and inferior surface of tongue of a SiGe/Si layered product, respectively (process S15). This SiGe/Si layered product was started along with the cutting plane line 6, and it was made to complete as diode 7 finally (process S16). The production number of the diode 7 at this time could be 50 pieces.
[0026] (Evaluation trial) The leakage current when applying a reverse bias to the produced diode 7 was measured, respectively. The leakage current is in the inclination which increases according to the electrical potential difference of a reverse bias, the electrical potential difference when the leakage current is set to 1mA here was defined as pressure-proofing of diode, and whether this electrical-potential-difference value is high or low estimated the size of the leakage current.
[0027] Consequently, pressure-proofing of 50 diodes 7 was 250V on the average. moreover, the case where 200V are made into a threshold -- total -- it became pressure-proofing beyond it. In addition, when unsettled, it became less than [100V] on the average. The average pressure-proofing at the time of not performing hydrofluoric acid processing (1st washing processing), but performing only vitriolization was set to 200V. Moreover, only in hydrofluoric acid processing, although average pressure-proofing was so much changeless with 200V, the clear defective with which pressure-proofing is less than 100V appeared 4%. Since the V-I property of seeming the effect of the movable ion by the metal impurity was observed when the property of this defective was analyzed, it was checked that the metal impurity is not fully removed.
[0028] (Example 2) The case where the diode of a different type from the above as a semiconductor device of an example 2 is produced is explained with reference to drawing 2 .
[0029] The Si substrate 1 of n mold of 15ohms of membrane resistance cm was prepared (process S21). Laminating formation of the SiGe film 2 of p mold was carried out on this n mold Si substrate 1 at 0.4 micrometers in thickness (process S22). A chemical-vapor-deposition method like CVD was used for membrane formation of this p mold SiGe film 2. Concentration of p mold dopant in the SiGe film 2 was made into 1017cm - three sets. Moreover, germanium concentration in the SiGe film 2 was made into pentatomic %.
[0030] subsequently, parts other than the part which it leaves as diode -- laws, such as dry etching or wet etching, -- by removing using a method, punching processing of a predetermined pattern was performed on the SiGe film 2, and many substrate exposures 3 were formed. These substrate outcrops 3 set the path to 1mm, and set 30 micrometers and mutual pitch spacing to 1.5-5mm for the depth. Furthermore, it was immersed in the solution with which 48% water solution of fluoric acid, 70% water solution of nitric acids, and pure water were mixed at a rate of 1:1:10 for about 20 seconds, and surface etching was performed (process S23).
[0031] Then, after immersing the SiGe/Si layered product into the hydrofluoric acid solution and performing 1st washing processing, it rinsed and dried, the SiGe/Si layered product was immersed into the sulfuric-acid solution, and 2nd washing processing was performed (process S24). The hydrofluoric acid solution used for the 1st washing processing dilutes the hydrofluoric acid of 48 mass % concentration to 1/50 with water. The sulfuric-acid solution used for the 2nd washing processing prepares a sulfuric-acid 96 mass % water solution and a hydrogen-peroxide-solution 48 mass % solution at a rate of 1:2.
[0032] Then, laminating formation of the metal electrodes 4 and 5 was carried out with the vacuum deposition method on the top face and inferior surface of tongue of a SiGe/Si layered product,

respectively (process S25). This SiGe/Si layered product was started along with the cutting plane line 6 (process S26). Then, the started SiGe/Si layered product was completed using the silicone gel by the Shin-etsu silicone company as an insulating material 8 as diode 7 by which the covering insulation was covered and carried out in the front face (process S27). The production number of the diode 7 at this time could be 20 pieces.

[0033] (Evaluation trial) The leakage current when applying a reverse bias to the produced diode 7 was measured, respectively. Evaluation conditions presupposed that it is the same as the above-mentioned example 1. Consequently, average pressure-proofing was set to 280V. Moreover, the following [200V] did not appear for the diode of an example 2. As a result of investigating pressure-proofing about the diode when not performing covering by surface etching and silicone gel as an example of a comparison, the average pressure-proofing was 250V. The effectiveness of the approach performed by this example 2 from now on was checked.

[0034]

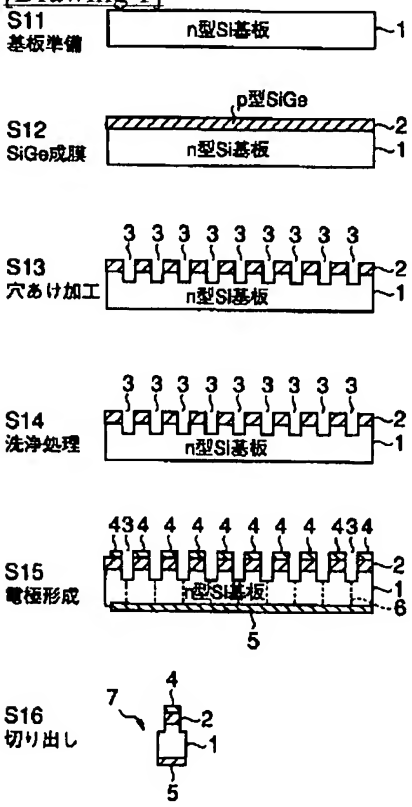
[Effect of the Invention] According to this invention, generating of the leakage current in a SiGe/Si heterojunction interface is prevented effectively. For this reason, upgrading of semiconductor devices, such as diode with a SiGe/Si heterojunction interface and a bipolar transistor, is planned, and the yield improves, and the application of the SiGe mixed-crystal film is expanded as that result.

[Translation done.]

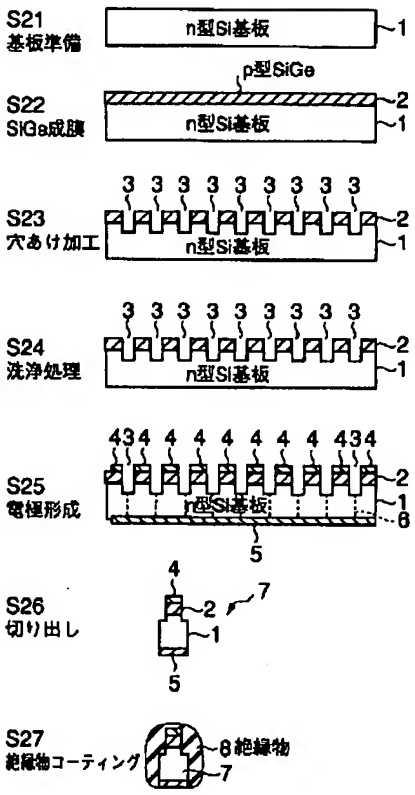
* NOTICES *

DRAWINGS

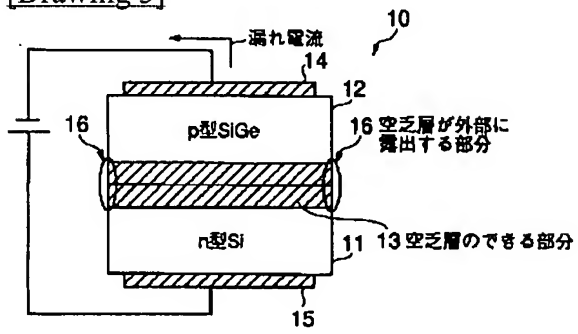
[Drawing 1]



[Drawing 2]



[Drawing 3]



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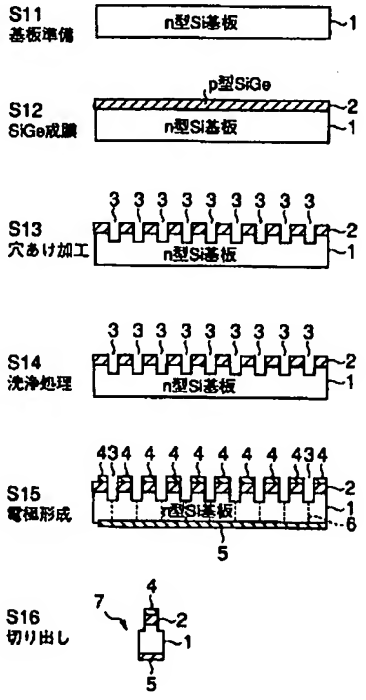
(54)【発明の名称】　半導体装置の作製方法

(57)【要約】
【課題】　ＳｉＧｅ／Ｓｉヘテロ接合界面に漏れ電流を生じない半導体装置の作製方法を提供する。
【解決手段】　第１導電型のＳｉＧｅと第２導電型のＳｉ又はＳｉＧｅとが相互接触する接合界面を有する半導体装置の作製方法において、前記接合界面が表面に露出する部分を、弗化水素酸を含む溶液で洗浄し、その後、硫酸を含む溶液で洗浄する。



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【特許請求の範囲】
【請求項１】　第１導電型のＳｉＧｅと第２導電型のＳｉ又はＳｉＧｅとが相互接触する接合界面を有する半導体装置の作製方法において、
前記接合界面が表面に露出する部分を、弗化水素酸を含む溶液で洗浄し、その後、硫酸を含む溶液で洗浄することを特徴とする半導体装置の作製方法。
【請求項２】　第１導電型のＳｉＧｅと第２導電型のＳｉ又はＳｉＧｅとが相互接触する接合界面を有する半導体装置の作製方法において、
前記接合界面が表面に露出している部分をエッチングし、次いで、弗化水素酸を含む溶液で洗浄し、その後、硫酸を含む溶液で洗浄し、次いで前記接合界面が表面に露出している部分に絶縁物を被覆することを特徴とする半導体装置の作製方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明はＳｉＧｅを用いたダイオードやトランジスタのような半導体装置を製造する半導体装置の製造方法に関する。
【０００２】
【従来の技術】ＳｉＧｅ混晶膜は、Ｓｉと接合させた電子デバイス、例えばｎ型Ｓｉ－ｐ型ＳｉＧｅ－ｎ型Ｓｉを順次接合した構造、すなわちヘテロ接合型バイポーラトランジスタとすることで、Ｓｉのみの構造と比べて高周波特性に優れたトランジスタを実現することができるので、今日では高周波用途の集積回路に広く普及している。また、本発明者は、ｐ型ＳｉＧｅとｎ型またはｎ⁻型のＳｉとを接合したダイオードでは従来のＳｉダイオードに比べて順方向から逆方向にバイアス転換したときのリカバリ時間が短く、高速動作が可能であることを、先の特願２０００－０４４３０６号の出願明細書及び図面において明らかにした。
【０００３】このような特性のＳｉＧｅ混晶膜を利用したヘテロ接合型トランジスタやダイオードにおいて、耐電圧特性を高めることは歩留まり向上の観点と用途拡大の観点とから製造者間で強く要望されている。このため、耐圧のかかる近傍部位のダイオード構造、すなわちｐ型ＳｉＧｅとｎ型Ｓｉとを接合した構造、あるいはｎ型ＳｉＧｅとｐ型Ｓｉとを接合した構造、これらを総称して以下ＳｉＧｅ／Ｓｉダイオードと呼ぶこととするが、このＳｉＧｅ／Ｓｉダイオードではｐｎ接合界面での逆バイアスのときの漏れ電流が問題となる。
【０００４】
【発明が解決しようとする課題】従来のＳｉＧｅ／Ｓｉダイオードに生じる漏れ電流について図３を参照して説明する。図３はＳｉＧｅ／Ｓｉダイオード１０に逆バイアスをかけたときに生じる漏れ電流を模式的に示した図である。ダイオード１０に逆バイアスをかけると、図示のようにｐｎ接合界面のところに空乏層１３ができ、この空乏層１３に電界が集中する。ｐｎ接合界面にはダイオードの外部に露出する部分１６が存在し、この露出部分１６での空乏層はそれ以外のところの空乏層に比べて幅が狭くなる傾向にある。そのため、この露出部分１６での電界集中の度合いが高くなり、ダイオードに生じる漏れ電流は露出部分１６の物質状態に強く支配されることとなる。

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【０００５】ここで、漏れ電流を支配する露出部分１６の物質状態とは、具体的には露出部分１６における結晶欠陥、空気放電、および不純物の３つである。このうち結晶欠陥は、各半導体層の作製プロセスに依存しており、半導体作製プロセスの品質管理には可能な限り結晶欠陥が入らないように十分な注意が払われているので、通常の場合は単独では無視できないほどの有害な欠陥に成長するまでには至らない。また、空気放電に関してはそれが起こらないように、例えば特願２０００－０２５４２８号の出願明細書及び図面に記載の先行技術ではシリコーンジェルなどの絶縁物で表層を覆うなどの対処がなされている。
【０００６】しかし、不純物については前二者のように有効な対処方法がこれまで未だ明らかにされていない。漏れ電流の誘因となりうる不純物元素にはＮａ，Ｋ，Ｆｅ，Ａｕなどの金属類、またハイドロカーボンなどの大気や水洗時に付着する不純物などがある。また、露出部分１６が酸化されて表面にＧｅ酸化物が生成されると、この酸化物も漏れ電流の原因となる。したがって、漏れ電流を低く抑えるためには、露出部分１６において、結晶欠陥を抑え、かつ空気放電を抑えた上に、さらに漏れ電流を誘起する有害な不純物を十分少なくする処理が要求される。
【０００７】ところで、全てＳｉで構成される従来のダイオードにおいては、ｐｎ接合の露出部分を熱酸化処理するのが一般的である。これは９００℃以上の高温の酸素又は水蒸気の雰囲気下でダイオードの表面を酸化する方法であり、この熱酸化処理を行うと、露出部分のＳｉが酸化されて絶縁化し、これにより漏れ電流が減少する。このような熱酸化法は、金属不純物には無力であるが、Ｓｉ系のデバイスでは有効であり、これまでにも頻繁に利用されている。
【０００８】しかし、従来の熱酸化法をＳｉＧｅ／Ｓｉダイオードにそのまま適用すると、ＳｉＧｅの表層でできる酸化層とＳｉＧｅとの界面の部分にＧｅの偏析が起こり、これが漏れ電流の原因となる。このため、熱酸化法をＳｉＧｅに適用するためにはＧｅが偏析を起こさない酸化条件の丹念な探索研究が必要であるが、その有効な方策は現在に至るまで未だ報告が見られず、未解決のまま残されている。
【０００９】なお、上記従来技術の問題点はＳｉＧｅ／Ｓｉダイオードのヘテロ接合界面に関するものであるが、ＳｉＧｅ／ＳｉＧｅダイオードでも同様の問題を生

じている。

【００１０】本発明は上記の課題を解決するためになされたものであって、ＳｉＧｅ／Ｓｉヘテロ接合界面又はＳｉＧｅ／ＳｉＧｅヘテロ接合界面、特にその露出面に漏れ電流を生じない半導体装置の作製方法を提供することを目的とする。

【００１１】

【課題を解決するための手段】本発明に係る半導体装置の作製方法は、第１導電型のＳｉＧｅと第２導電型のＳｉ又はＳｉＧｅとが相互接触する接合界面を有する半導体装置の作製方法において、前記接合界面が表面に露出する部分を、弗化水素酸を含む溶液で洗浄し、その後、硫酸を含む溶液で洗浄することを特徴とする。

【００１２】また、本発明に係る半導体装置の作製方法は、第１導電型のＳｉＧｅと第２導電型のＳｉ又はＳｉＧｅとが相互接触する接合界面を有する半導体装置の作製方法において、前記接合界面が表面に露出している部分をエッチングし、次いで、弗化水素酸を含む溶液で洗浄し、その後、硫酸を含む溶液で洗浄し、次いで前記接合界面が表面に露出している部分に絶縁物を被覆することを特徴とする。

【００１３】ＳｉＧｅ／Ｓｉダイオードの接合界面の表面露出部分は、大気中に放置しておくと自然に酸化してしまう。このとき、大気中からの不純物（ハイドロカーボンなど）の吸着、また作業者が素手などで接触することによってもたらされる金属（Ｎａ，Ｋ）イオンなどの混入、さらに酸化されてできるＧｅの酸化物（GeO_2）などが不純物として想定される。これらの不純物は漏れ電流を引き起こし、半導体装置の耐圧特性を低下させる。

【００１４】本発明において、先ず弗化水素酸を含む溶液にＳｉＧｅ／Ｓｉダイオードを浸すのは、該露出部分にできる酸化物を取り除くためである。酸化層として数μｍ程度の厚さでも弗化水素酸溶液に浸す時間を変えることで、容易に取り除くことができる。この洗浄処理により露出部分の表面では接合界面は水素終端される。しかし、この工程ではハイドロカーボンや金属不純物は除去されない。

【００１５】次いで、ＳｉＧｅ／Ｓｉダイオードを硫酸含有水溶液に浸すと、金属不純物とハイドロカーボンが溶液に溶け出て、表層から取り除かれる。この際に表層は１ｎｍ（１０Å）程度の厚さで酸化されるが、この際作られるのはSiO_2のみでＧｅの酸化物（GeO_2）は作られない。硫酸の影響で表層のＧｅ原子は酸化するが、Ｇｅ酸化物は硫酸の溶液に溶けるため、表層にGeO_2として残らない。ここでできた表層の状態は、金属、ハイドロカーボン、Ｇｅ酸化物などの不純物が低く抑えられるほか、表層にＳｉ酸化物が薄くでき、これが外界からの不純物にたいして不活性であり、その後の不純物吸着を抑える働きがある。

【００１６】本発明では弗化水素酸処理と硫酸処理を順次行うが、どちらか一方が欠けた場合には本発明の効果は発現しない。弗化水素酸処理が欠けた場合は、表層の自然酸化膜が厚いときに自然酸化膜中のGeO_2の除去が不十分になるとともに、自然酸化膜中にある金属不純物を除去できない。一方、硫酸処理が欠けた場合は、弗化水素酸処理でとりきれない金属不純物とハイドロカーボンが残留することになる。また、これら弗化水素酸処理と硫酸処理とを逆にした場合は、表面が水素終端で終わるため、表面が酸化膜で終わる本発明に比べてその後の不純物吸着を抑える効果が弱くなる。

【００１７】ＳｉＧｅ／Ｓｉダイオードにおいて逆バイアス時の漏れ電流の原因は、上述したように接合界面の表面露出部分での、1)結晶欠陥、2)空気放電、3)不純物である。

【００１８】第１の発明は表層の不純物を効果的に除去する方法であるが、これに第２の発明のように1)結晶欠陥と2)空気放電を除去する工程を付加することで、さらに漏れ電流の少ないダイオードとなる。

【００１９】具体的には、半導体表面部分の結晶欠陥の除去のために、化学エッチング、例えばＫＯＨなどのアルカリ系水溶液か弗酸と硝酸の混合水溶液などで表層をエッチングすることで取り除く。これにより引っかき傷やプラズマなどの処理による表面損傷による結晶欠陥を取り除くことができる。その後に、不純物を除去するために、第１の発明で示した弗化水素酸溶液と硫酸溶液に順次浸漬して洗浄する。その後、表面を絶縁物で覆うことで空気との接触を防止するようにする。これら３つの方策を組み合わせることで、漏れ電流による性能劣化の少ないＳｉＧｅ／Ｓｉダイオードを得ることができる。

【００２０】上記方策はＳｉＧｅ／Ｓｉダイオードの例について説明しているが、ＳｉＧｅ／ＳｉＧｅダイオードでも同様の効果を得ることができる。

【００２１】

【発明の実施の形態】以下、添付の図面を参照して本発明の様々な好ましい実施例について説明する。

【００２２】（実施例１）実施例１の半導体装置としてｐ－ＳｉＧｅ／ｎ－Ｓｉ接合型ダイオードを作製した。その作製方法について図１を参照して説明する。膜抵抗１５Ωｃｍのｎ型のＳｉ基板１を準備した（工程Ｓ１１）。このｎ型Ｓｉ基板１の上にｐ型のＳｉＧｅ膜２を厚さ０．４μｍに積層形成した（工程Ｓ１２）。このｐ型ＳｉＧｅ膜２の成膜にはＣＶＤのような化学気相堆積法を用いた。ＳｉＧｅ膜２中のｐ型ドーパントの濃度は10^{17} cm^{-3}台とした。また、ＳｉＧｅ膜２中のＧｅ濃度は５原子％とした。

【００２３】次いで、ダイオードとして残す部分以外の部分を乾式エッチング又は湿式エッチングなどの定法を用いて除去することにより、ＳｉＧｅ膜２に所定パターンの穴あけ加工を行い、多数の基板露出面３を形成した

（工程Ｓ１３）。これらの基板露出部３は、幅を１ｍｍ、深さを３０μｍ、相互間のピッチ間隔を１．５～５ｍｍとした。

【００２４】その後、弗化水素酸溶液中にＳｉＧｅ／Ｓｉ積層体を浸漬して第１の洗浄処理を行った後に、水洗、乾燥し、硫酸溶液中にＳｉＧｅ／Ｓｉ積層体を浸漬して第２の洗浄処理を行った（工程Ｓ１４）。第１の洗浄処理に用いた弗化水素酸溶液は、４８質量％濃度の弗化水素酸を水で１／５０に希釈したものである。第２の洗浄処理に用いた硫酸溶液は、硫酸９６質量％水溶液と過酸化水素水４８質量％溶液を１：２の割合で調合したものである。

【００２５】この後、ＳｉＧｅ／Ｓｉ積層体の上面と下面に金属電極４，５を真空蒸着法によりそれぞれ積層形成した（工程Ｓ１５）。このＳｉＧｅ／Ｓｉ積層体を切断線６に沿って切り出し、最終的にダイオード７として完成させた（工程Ｓ１６）。このときのダイオード７の作製個数は５０個とした。

【００２６】（評価試験）作製したダイオード７に逆バイアスをかけたときの漏れ電流をそれぞれ計測した。漏れ電流は逆バイアスの電圧に応じて増加する傾向にあり、ここでは漏れ電流が１ｍＡになったときの電圧をダイオードの耐圧として定義し、この電圧値が高いか低いかで漏れ電流の大小を評価した。

【００２７】その結果、５０個のダイオード７の耐圧は平均で２５０Ｖであった。また、２００Ｖを閾値とした場合に、全数それ以上の耐圧となった。なお、未処理の場合は平均で１００Ｖ以下となった。弗化水素酸処理（第１の洗浄処理）を行わず、硫酸処理のみを行った場合の平均耐圧は２００Ｖとなった。また、弗化水素酸処理のみでは平均耐圧は２００Ｖとそれほど変化はないが、耐圧が１００Ｖを下回る明らかな不良品が４％出現した。この不良品の特性を解析したところ、金属不純物による可動イオンの影響と思われるＶ－Ｉ特性が観測されたことから、金属不純物が十分に除去されていないことが確認された。

【００２８】（実施例２）実施例２の半導体装置として上記とは異なるタイプのダイオードを作製する場合について図２を参照して説明する。

【００２９】膜抵抗１５Ωｃｍのｎ型のＳｉ基板１を準備した（工程Ｓ２１）。このｎ型Ｓｉ基板１の上にｐ型のＳｉＧｅ膜２を厚さ０．４μｍに積層形成した（工程Ｓ２２）。このｐ型ＳｉＧｅ膜２の成膜にはＣＶＤのような化学気相堆積法を用いた。ＳｉＧｅ膜２中のｐ型ドーパントの濃度は10^{17} cm^{-3}台とした。また、ＳｉＧｅ膜２中のＧｅ濃度は５原子％とした。

【００３０】次いで、ダイオードとして残す部分以外の部分を乾式エッチング又は湿式エッチングなどの定法を用いて除去することにより、ＳｉＧｅ膜２に所定パターンの穴あけ加工を行い、多数の基板露出面３を形成した。これらの基板露出部３は、径を１ｍｍ、深さを３０μｍ、相互間のピッチ間隔を１．５～５ｍｍとした。さらに、弗酸４８％水溶液と硝酸７０％水溶液と純水とを１：１：１０の割合で混合させた溶液に約２０秒間浸漬して表面エッチングを行った（工程Ｓ２３）。

【００３１】その後、弗化水素酸溶液中にＳｉＧｅ／Ｓｉ積層体を浸漬して第１の洗浄処理を行った後に、水洗、乾燥し、硫酸溶液中にＳｉＧｅ／Ｓｉ積層体を浸漬して第２の洗浄処理を行った（工程Ｓ２４）。第１の洗浄処理に用いた弗化水素酸溶液は、４８質量％濃度の弗化水素酸を水で１／５０に希釈したものである。第２の洗浄処理に用いた硫酸溶液は、硫酸９６質量％水溶液と過酸化水素水４８質量％溶液を１：２の割合で調合したものである。

【００３２】この後、ＳｉＧｅ／Ｓｉ積層体の上面と下面に金属電極４，５を真空蒸着法によりそれぞれ積層形成した（工程Ｓ２５）。このＳｉＧｅ／Ｓｉ積層体を切断線６に沿って切り出した（工程Ｓ２６）。その後、切り出したＳｉＧｅ／Ｓｉ積層体を絶縁物８としての信越シリコーン社製のシリコーンジェルを用いて表面を被覆し、被覆絶縁されたダイオード７として完成させた（工程Ｓ２７）。このときのダイオード７の作製個数は２０個とした。

【００３３】（評価試験）作製したダイオード７に逆バイアスをかけたときの漏れ電流をそれぞれ計測した。評価条件は上記実施例１と同じとした。その結果、平均耐圧は２８０Ｖとなった。また、実施例２のダイオードでは２００Ｖ以下のものは出現しなかった。比較例として表面エッチングとシリコーンジェルによる被覆を行わない場合のダイオードについて耐圧を調べた結果、その平均耐圧は２５０Ｖであった。これから本実施例２でおこなった処理法の有効性が確認された。

【００３４】

【発明の効果】本発明によれば、ＳｉＧｅ／Ｓｉヘテロ接合界面における漏れ電流の発生が有効に防止される。このため、ＳｉＧｅ／Ｓｉヘテロ接合界面をもつダイオードやバイポーラトランジスタ等の半導体装置の品質向上が図られ、また歩留まりが向上し、その結果としてＳｉＧｅ混晶膜の用途が拡大する。

【図面の簡単な説明】

【図１】本発明の第１の実施形態に係る半導体装置の作製方法を示すフローチャート。

【図２】本発明の第２の実施形態に係る半導体装置の作製方法を示すフローチャート。

【図３】従来の半導体装置を示す断面模式図。

【符号の説明】

１…ｎ型Ｓｉ基板、

２…ｐ型ＳｉＧｅ、

３…エッチング除去部（基板露出部）、

４，５…電極、

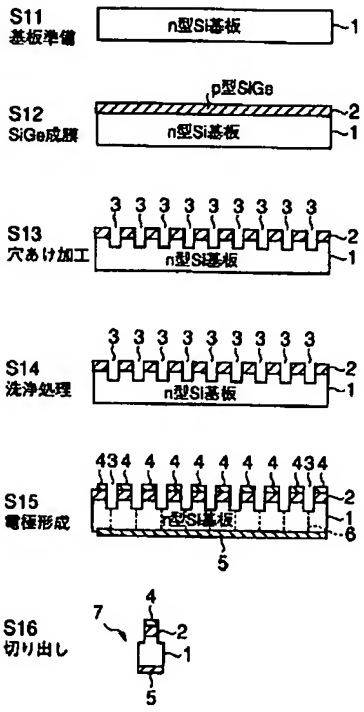
7

6…切断線、
7…半導体装置（ダイオード）、
8…被覆絶縁物、

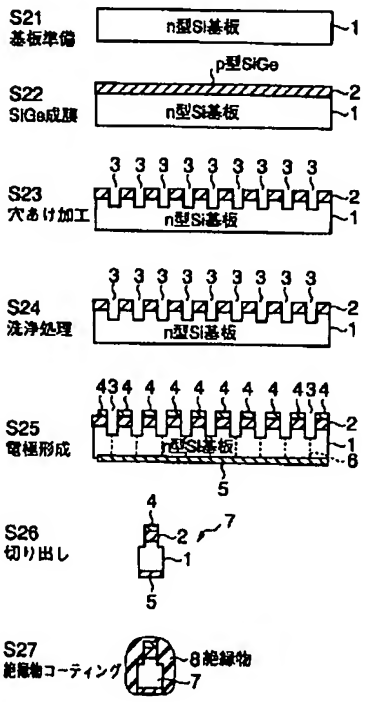
8

１３…空乏層（接合界面を含む近傍部位）、
１６…露出部分（空乏層が外部に露出する部分）。

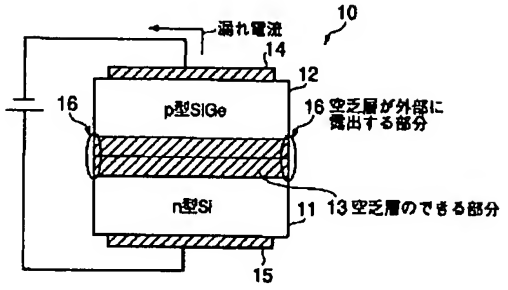
【図１】



【図２】



【図３】



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